PROJECT RESULT

Enabling
IC technologies
for applications

MEDEA+

T104: Safe IC design for robust applications (SIDRA)

Chip-level design simulation improves electrostatic discharge robustness

Electrostatic discharge (ESD) is a major concern when designing ever smaller electronic devices. The MEDEA+ SIDRA project has developed design-simulation methods for the protection of mixed signal integrated circuits against ESD damage at chip level – particularly important with the trend to complete system-on-chip devices. As a consequence, design times can be cut, redesigns avoided, productivity increased and reliability improved. The results in terms of guaranteed ESD robustness and quality are already being exploited by European chipmakers to safeguard their positions in a tough global market.

Electrostatic discharge damage is an increasing challenge in microelectronics. Smaller critical dimensions on integrated circuit (IC) chips mean lower breakdown voltages for PN junctions and thinner gate oxides compared with older processes and technologies. And this will be a greater problem in the future as device geometries continue to shrink.

Such ESD problems are found in all types of application – from the fast increasing use of electronics in vehicles for safety-critical control and entertainment systems to consumer electronics, security devices, wireless and mobile communications, and chip-equipped smart cards. It is particularly important to ensure ESD robustness and quality in complete system-on-chip (SoC) devices to avoid in-use failures and field returns.

The MEDEA+ T104 SIDRA project set out to develop and verify simulation-guided design methodologies for protection at chip level to prevent weakness of ICs subject to fast transient pulses. Work centred on the use of the charge-device model (CDM) that allows very high currents, up to 10 A, with extremely fast pulses – durations less than 2 ns. And SIDRA built on the results of the earlier MEDEA+ ASDESE project on device-level ESD protection. Project partners comprised major European chipmakers, research institutes, universities and a software house. These partners had already been involved in ASDESE, where they experienced very good co-operation. SIDRA was seen as an essential continuation and was carried out within the MEDEA+ framework because of the possibility of working with a wide range of European partners and the benefit of exchanging results through the MEDEA forums.

Protection at full chip level

The primary objective was to ensure ESD protection at the full chip level, not previously tackled. The partners focused on mixed signal ICs such as in automotive applications. These are subject to extremely tough specifications due to their safety-critical functions, the hostile environment and the high degree of heterogeneous complexity involving sensitive analogue, power and digital control elements. Chips for other critical applications such as identification and platform security face similar requirements.

Simulation methods were investigated with the development of the necessary characterisation techniques. The institutes and universities involved contributed the crucial knowledge of innovative characterisation methods:

- TU Vienna focused on optical measurement, developing the more sensitive transient interferometric mapping (TIM) measurement method that localises stressed

regions within the silicon during ESD. TIM has been tested successfully by the industrial partners in SIDRA; and

- Fraunhofer IZM in Munich – as a subcontractor of several partners – developed advanced measurement methods such as ultra fast transmission line pulse (TLP), transient latch-up (TLU) and capacitive-coupled TLP (cc-TLP).

All these new characterisation methods were published and have been well received by the microelectronics industry. Moreover, they have contributed directly to standardisation progress. SIDRA members used the project results as their contribution to global standardisation activities, particularly in the Electrostatic Discharge Association (ESDA) workgroup dealing with CDM, TLP and TLU issues.

Guaranteeing performance

The technology suppliers carried out measurements to verify the results of full chip simulations that took account of parasitic resistances and capacitances of the package, substrate and power supply to predict CDM weaknesses in the design before production. One of the most innovative outcomes has been the conclusion of design guidelines depending on the technologies used to guarantee CDM robustness for future designs in general.

From the beginning, partners developed a common set of test structures to cover the wide range of technologies in which they were involved, making it possible to exchange know how and results despite their different applications. SIDRA covered advanced technologies in the field of smart power 0.35 µm bipolar CMOS-DMOS (BCD) technology with 7 nm gate oxides, 90 nm and 65 nm CMOS technology and two different silicon-on-insulator (SOI) technologies.

Single ESD-protection elements, small protection circuits and more complex full chip level simulation of a demonstrator circuit were successfully developed and performed. The results matched up well to the measured silicon and the project achieved the objective, making it possible to provide a simulation setup for pre-emptive CDM investigations of ESD protection elements and to deduce design guidelines for future applications.

By simulating CDM stresses, it is possible to optimise ESD protection before initial chip fabrication – avoiding redesigns and so saving development time and costs. In addition, good qualification of circuit libraries now makes it possible to guarantee robustness for the next products in these technologies – ensuring better quality for customers.

Keeping Europe ahead

Results of this project are enabling European chipmakers to offer top-level design kits for ESD and TLU, keeping the industry at the leading edge in the tough global market for semiconductor devices and safeguarding high level jobs in Europe.

SIDRA outcomes will have a particular impact in the crucial automotive electronics area where safety and reliability of equipment are paramount with very challenging target values for failure rates. The design simulation technologies are already being offered to customers to meet ever tougher specifications in ever more sensitive technologies.

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PARTNERS:

Atmel Germany
ETH Zurich
Infineon Technologies
NXP (formerly Philips Semiconductors)
Robert Bosch
STMicroelectronics
TU Vienna (ISSE)
X-FAB

PROJECT LEADER:

Petra Rose
Robert Bosch

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COUNTRIES INVOLVED:

Austria
Germany
Italy
The Netherlands
Switzerland

MEDEA+

MEDEA+ Office
140bis, Rue de Rennes
F-75006 Paris
France
Tel.: +33 1 40 64 45 60
Fax: +33 1 40 64 45 89
Email: medeaplus@medeaplus.org
http://www.medeaplus.org

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.